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Box Patent Application

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Enclosed herewith for filing is a patent application, as follows:

Inventor(s): Adrian E. Ong
Title: Controlling The Set Up Of A Memory Address

- 4 Sheets of drawings
- 20 page Specification ☒ and Title Page
- 4 pages of Claims
- 1 page Abstract
- 2 page Declaration/Power of Attorney (signed)
- ☒ 1 page(s) Assignment
- ☒ 1 page(s) Recordation Cover Sheet
- ☐ page(s) PTO Form 1449
- ☐ Copies of Cited References
- ☒ Small Business Concern Declaration (2 pages)
- ☐ Independent Inventor's Declaration
- ☐ Certified copy of _____ Application
- ☐ Other: _____

CLAIMS AS FILED (fees computed under §1.9(f))

For	Number Filed		Number Extra		Rate	\$	Basic Fee
							395.00
Total Claims	10	-20 =	0	x	\$11	= \$	0.00
Independent Claims	2	-3 =	0	x	\$41	= \$	0.00
<input type="checkbox"/> Application contains one or more multiple dependent claims (\$135 total fee)						\$	0.00

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Respectfully submitted,

Philip W. Woo
Philip W. Woo
Attorney for Applicant(s)
Reg. No. 39,880

CONTROLLING THE SET UP OF A MEMORY ADDRESS

Adrian E. Ong

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FIELD OF THE INVENTION

The present invention relates generally to the field of semiconductor integrated circuits, and more particularly, to controlling the set up of a memory address.

BACKGROUND OF THE INVENTION

Integrated circuit (IC) memory devices allow large amounts of data to be stored in relatively small physical packages. A typical IC memory device comprises a plurality of memory cells. Separate bits of data may written into, stored, and read out of each of these memory cells. Memory cells can be organized in rows, each of which may be identified by a respective address. A respective row line or "word line" provides access to each row of memory cells. For this access, each word line is "enabled" by latching and decoding the address for the respective row.

According to a previously developed technique, a row address strobe (RAS) signal is exclusively used to set up each row address so that such address can be latched for decoding. With such prior technique, a new
5 row address cannot be set up until a previous row address has been completely decoded. This limits the speed at which an IC memory device can be operated. An ongoing challenge for IC devices in general, however, is to increase performance by providing more rapid
10 operation. Thus, it is desirable that the addressing of a row be made more rapid.

SUMMARY

The disadvantages and problems associated with
15 previously developed techniques for setting up a row address have been substantially reduced or eliminated using the present invention.

In accordance with one embodiment of the present invention, a circuit is provided for controlling the
20 set up of a memory address. The circuit includes a first latch circuit for latching a first memory address in response to a first simultaneous occurrence of a predetermined value for an output enable signal and a

predetermined value for a row address strobe signal. A second latch circuit is coupled to the first latch circuit. The second latch circuit receives the first memory address from the first latch circuit and latches
5 the first row address thereafter for decoding. The first latch circuit can latch a second memory address in response to a second simultaneous occurrence of the predetermined value for the output enable signal and the predetermined value for the row address strobe
10 signal, the second simultaneous occurrence occurring while the first row address is being decoded.

In accordance with another embodiment of the present invention, a method is provided for controlling the set up of a memory address. The method includes
15 the following: latching a first memory address in response to a first simultaneous occurrence of a predetermined value for an output enable signal and a predetermined value for a row address strobe signal; decoding the first memory address for access to at
20 least one memory cell corresponding to the first memory address; and while the first memory address is being decoded, latching a second memory address in response to a second simultaneous occurrence of the

predetermined value for the output enable signal and the predetermined value for the row address strobe signal.

An important technical advantage of the present invention includes providing more rapid operation of an IC memory device by controlling the set up of a memory address with both the row address strobe signal (RAS) and the output enable signal (\overline{OE}). This is accomplished by incorporating two latch circuits into the IC memory device. The first latch circuit stores or latches a first memory address upon the simultaneous occurrence of predetermined value for the \overline{OE} signal and a predetermined value for the RAS signal. The first memory address is then latched into the second latch circuit, where such address can be decoded for access into the respective memory cells. Upon the next simultaneous occurrence of the predetermined values for the \overline{OE} and RAS signals--which can take place while the first memory address is still being decoded--a second memory address is latched into the first latch circuit. Because the second memory address can be received and set up even as the first memory address is being

decoded, the present invention accelerates the operation of the IC memory device, thereby enhancing the device's performance.

Other important technical advantages of the present invention are readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

10 For a more complete understanding of the present invention and for further features and advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

15 Figure 1 is an exemplary block diagram of a circuit for controlling the set up of a memory address, in accordance with an embodiment of the present invention;

Figure 2 is an exemplary schematic diagram for the timing generator circuit shown in Figure 1, in accordance with an embodiment of the present invention;

Figure 3 is an exemplary schematic diagram for the first latch circuit and the second latch circuit shown

in Figure 1, in accordance with an embodiment of the present invention; and

Figure 4 is an exemplary timing diagram for a memory device wherein the set up of a memory address is controlled in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention and their advantages are best understood by referring to Figures 1 through 4 of the drawings. In these drawings, like numerals are used for like and corresponding parts.

Figure 1 is an exemplary block diagram of a circuit 10 for controlling the set up of a memory address, in accordance with an embodiment of the present invention. Circuit 10 can be incorporated into any suitable integrated circuit (IC) memory device for enhancing performance thereof. For example, in one embodiment, such memory device may be a dynamic random access memory (DRAM) in which data stored therein decays over time; accordingly, numerous refresh

operations are required to maintain the integrity of the stored data. Such DRAM can be asynchronous.

Circuit 10 receives an address (ADDR) signal, which conveys information relating to one or more
5 memory addresses for rows--or alternatively, columns--of memory cells to be accessed. In general, as used herein, "memory address" can be either a row address or a column address. Although the following describes the invention primarily with regard to row addresses, it
10 should be understood that the invention may be equally applicable to column addresses.

A buffer 12 buffers and inverts the ADDR signal. Buffer 12 is enabled by a power-up row address ($\overline{\text{PROW}}$) signal, which is generated by a timing generator
15 circuit 14 coupled to the buffer. As used herein, the terms "coupled," "connected," or any variant thereof, means any coupling or connection, either direct or indirect, between two or more elements.

Timing generator circuit 14 operates on an output
20 enable ($\overline{\text{OE}}$) signal and a row address strobe (RAS) signal to generate timing signals $\Phi 1$ and $\overline{\Phi 1}$, as well as the $\overline{\text{PROW}}$ signal. In general, the value (high or low)

for each of the $\Phi 1$, $\overline{\Phi 1}$, and $\overline{P\overline{R}O\overline{W}}$ timing signals may depend on the values of the $\overline{O\overline{E}}$ and RAS (or a row address strobe complement ($\overline{R\overline{A}S}$)) signals. In one embodiment, the $\overline{P\overline{R}O\overline{W}}$, $\Phi 1$ and $\overline{\Phi 1}$ signals may each

5 comprise pulse signals which are generated in response to the simultaneous occurrence of a predetermined value for the $\overline{O\overline{E}}$ signal and a predetermined value for the RAS signal. For example, as described herein, the simultaneous occurrence of a high value for the $\overline{R\overline{A}S}$

10 signal and a low value for the $\overline{O\overline{E}}$ signal causes a pulse in the $\Phi 1$ signal. Specifically, such pulse in the $\Phi 1$ signal may be generated when the value of the $\overline{R\overline{A}S}$ signal is high as the value of the $\overline{O\overline{E}}$ signal goes low, or alternatively, when the value of the $\overline{O\overline{E}}$ signal

15 is low as the value of the $\overline{R\overline{A}S}$ signal goes high. An exemplary derivation of the $\Phi 1$, $\overline{\Phi 1}$, and $\overline{P\overline{R}O\overline{W}}$ timing signals from the $\overline{O\overline{E}}$ and RAS (or $\overline{R\overline{A}S}$) signals is described below in more detail.

A first latch circuit 16 and a second latch

20 circuit 18 are coupled in series to the output lead of buffer 12. First latch circuit 16 receives, and

responds to, the $\Phi 1$ and $\overline{\Phi 1}$ signals. First latch circuit 16 passes and latches a memory address (conveyed by the ADDR signal) upon the occurrence of a pulse in the $\Phi 1$ signal. In one embodiment, as
5 described herein, for the duration of a pulse in the $\Phi 1$ signal, first latch circuit 16 passes a memory address; at the end of such pulse in the $\Phi 1$ signal, first latch circuit 16 latches the memory address.

An input lead of second latch circuit 18 is
10 connected to the output lead of first latch circuit 16 so that second latch circuit 18 may receive memory addresses therefrom. Second latch circuit 18 receives a $\Phi 2$ signal and its complement, $\overline{\Phi 2}$. In one embodiment, the $\Phi 2$ and $\overline{\Phi 2}$ signals may comprise a
15 number of pulse signals. Second latch circuit 18 passes and latches a memory address upon the occurrence of a pulse in the $\Phi 2$ signal. For example, in one embodiment, for the duration of a pulse in the $\Phi 2$ signal, second latch circuit 18 passes a memory
20 address; at the end of such pulse in the $\Phi 2$ signal, second latch circuit 18 latches the memory address. When passed by and/or latched in second latch circuit

18, a memory address can be decoded for access into the corresponding memory cells.

A first stage row decode circuit 20 and a second stage row decode circuit 22 are coupled in series to the output lead of second latch circuit 18. First and second stage row decode circuits 20 and 22 decode, process, or otherwise operate upon a memory address so that the respective memory cells can be accessed for reading and writing. The implementation of first and second stage row decode circuits 20 and 22 is readily understood by those of ordinary skill in the art.

In operation, the ADDR signal (conveying the addresses for rows of memory cells) is buffered and inverted by buffer 12 when a low value on the $\overline{\text{PROW}}$ signal is output by timing generator circuit 14. First latch circuit 16 passes and latches a first memory address when a pulse appears in the $\Phi 1$ signal, which coincides with the simultaneous occurrence of a predetermined value for the RAS (or $\overline{\text{RAS}}$) signal and a predetermined value for the $\overline{\text{OE}}$ signal. In one embodiment, this may occur when the value of the RAS signal is low (and the $\overline{\text{RAS}}$ signal is high) and the

value of the \overline{OE} signal is low. While the first memory address is latched in first latch circuit 16, a pulse may appear in the $\Phi 2$ signal. This pulse causes the first memory address to be passed and latched by second latch circuit 18, where the such address can be decoded by first and second stage row decode circuits 20 and 22. At this point, even as the first memory address is being decoded, first latch circuit 16 can receive a second memory address conveyed in the ADDR signal.

Because circuit 10 can receive the next memory address before the first address is completely decoded, the operation of any memory device into which circuit 10 is incorporated is improved or enhanced.

Figure 2 is an exemplary schematic diagram for the timing generator circuit 14 shown in Figure 1, in accordance with an embodiment of the present invention. Figure 2 also illustrates circuitry for generating the \overline{OE} and RAS (and \overline{RAS}) signals.

The \overline{OE} signal is generated by a buffer 24 coupled in series to an inverter 26. Buffer 24 receives an external output enable (\overline{XOE}) signal at its input lead and is enabled by a power up (PWRUP) signal. Inverter

26 receives and inverts the output signal of buffer 24
to produce the $\overline{\text{OE}}$ signal. The RAS signal is generated
by series-connected inverters 28, 30, and 32. Inverter
28 is enabled by a power-up (PWRUP) signal and receives
5 an external row address strobe ($\overline{\text{XRAS}}$) signal at its
input lead. The output signal of inverter 28 is
received and inverted by inverter 30 to produce a row
address strobe complement $\overline{\text{RAS}}$ signal. The $\overline{\text{RAS}}$ signal
is inverted by inverter 32 to generate the RAS signal.

10 Timing generator circuit 14 comprises circuitry
for producing the $\Phi 1$ signal, the $\overline{\Phi 1}$ signal, and the
 $\overline{\text{PROW}}$ signal. As shown, timing generator circuit 14
includes a NOR gate 34 which receives the $\overline{\text{OE}}$ and RAS
signals at its input leads. A delay element 36 and an
15 inverter 38 are connected in series to the output lead
of NOR gate 34. A NAND gate 40 has input leads
connected to the output leads of NOR gate 34 and
inverter 38. NAND gate 40 outputs the $\Phi 1$ signal. An
inverter 40 receives the output signal of NAND gate 40
20 and outputs the $\overline{\Phi 1}$ signal. The operation of delay
element 36 and inverter 38 to delay the signal from NOR
gate 34 at one input of NAND gate 40 while the same

signal is immediately fed into the other input of NAND
gate 40 causes each of the $\Phi 1$ and $\overline{\Phi 1}$ signals to be a
pulse signal. A delay element 42 and an inverter 44
are also coupled in series to the output lead of NOR
5 gate 34. A NAND gate 46 receives the output signal of
NOR gate 34 and the output signal of inverter 44 and,
in response, generates the $\overline{P\text{ROW}}$ signal, which also can
be a pulse signal. The $\overline{P\text{ROW}}$ signal should be active
long enough for a valid memory address to feed through
10 the first latch circuit 16. Accordingly, a pulse in
the $\overline{P\text{ROW}}$ signal should be greater in duration than a
corresponding pulse in the $\Phi 1$ signal.

Figure 3 is an exemplary schematic diagram for
first latch circuit 16 and second latch circuit 18
15 shown in Figure 1, in accordance with an embodiment of
the present invention. As shown, first latch circuit
16 comprises a p-type transistor 48 and an n-type
transistor 50 coupled together at their sources and
drains. The gate of transistor 48 receives the $\Phi 1$
20 signal and the gate of transistor 50 receives the $\overline{\Phi 1}$
signal. In this arrangement, transistors 48 and 50
function as a passgate (implemented in CMOS) which

passes a buffered row address signal when the $\Phi 1$ signal goes low (and the $\overline{\Phi 1}$ signal goes high). The input lead for an inverter 52 is coupled to the output lead of the passgate formed by transistor 48 and 50. An inverter 54 is coupled at its input lead to the output lead of inverter 52, and at its output lead to the input lead of inverter 52. As such, inverters 52 and 54 function as a latch to hold a memory address.

Second latch circuit 18 comprises a p-type transistor 56, an n-type transistor 58, an inverter 60, and an inverter 62 coupled in substantially the same arrangement as transistor 48, transistor 50, inverter 52, and inverter 54 of first latch circuit 16. Moreover, these elements of second latch circuit 18 perform substantially the same functions (i.e., operate in substantially the same manner) as the comparable elements in first latch circuit 16. Specifically, transistors 56 and 58 operate as a passgate, which is triggered by a timing signal (in this case, the $\Phi 2$ signal). Inverters 60 and 62 operate as a latch to retain a memory address.

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In operation, upon the occurrence of a pulse in the $\Phi 1$ signal, the passgate formed by transistors 48 and 50 of first latch circuit 16 allows a first memory address to be latched by inverters 52 and 54. Upon the
5 occurrence of a pulse in the $\Phi 2$ signal, the passgate formed by transistor 56 and 58 in second latch circuit 18 passes the first memory address to inverters 60 and 62. Inverters 60 and 62 maintain this first memory address so that it may be operated upon or decoded. As
10 soon as the first memory address is latched into second latch circuit 18, first latch circuit 16 is available to receive a second memory address.

Figure 4 is an exemplary timing diagram 70 for a memory device wherein the setup of a memory address is
15 controlled in accordance with an embodiment of the present invention.

Timing diagram 70 includes a plurality of exemplary waveforms that may be input or generated for various signals appearing in the circuitry described
20 above with reference to Figures 1-3. Specifically, a row address strobe complement ($\overline{\text{RAS}}$) signal 72 can be output by inverter 30 of Figure 2. An output enable

($\overline{\text{OE}}$) signal 74 can be output by inverter 26 of Figure 2. An address (ADDR) signal 76 can be input into buffer 12 of Figure 1. A $\overline{\text{PROW}}$ signal 77 and a $\Phi 1$ timing signal 78 can be output by timing generator circuit 14 of Figures 1 and 2. A $\Phi 2$ timing signal 80 can be input into second latch circuit 18 of Figures 1 and 3.

ADDR signal 76 conveys information for a number of memory addresses which are represented by frames labeled "ROW" or "COLUMN" in signal 76. The set up of these memory addresses is controlled by $\overline{\text{RAS}}$ signal 72 and $\overline{\text{OE}}$ signal 74. That is, when a predetermined value for $\overline{\text{RAS}}$ signal 72 and a predetermined value for $\overline{\text{OE}}$ signal 74 simultaneously occur, a memory address is latched into first latch circuit 16 (Figure 1). In one embodiment, as depicted, this may occur when the value of $\overline{\text{RAS}}$ signal 72 is high and the value of $\overline{\text{OE}}$ signal 74 is low.

For example, in one period 82, a first row address is set up when the value of $\overline{\text{OE}}$ signal 74 is low as the value of $\overline{\text{RAS}}$ signal 72 transitions high. The

difference in time between the moment that \overline{OE} signal
74 goes low and the moment that \overline{RAS} signal 72 goes high
constitutes the \overline{OE} to \overline{RAS} setup time (t_{ORS}). The
difference in time between the moment that \overline{RAS} signal
72 goes high and the moment that \overline{OE} signal 74 goes
high again constitutes the \overline{OE} to \overline{RAS} hold time (t_{ORH}).
The difference in time between the beginning of the
first row address and the moment that \overline{RAS} signal 72
goes high constitutes the row address setup time (t_{ASR}).

10 The difference in time between the moment that \overline{RAS}
signal 72 goes high and the end of the first row
address constitutes the row address hold time (t_{RAH}).

During exemplary period 82, the transition of \overline{RAS}
signal 72 from low to high while \overline{OE} signal 74 is low
causes a pulse in $\Phi 1$ signal 78. During this pulse, $\Phi 1$
signal 78 is low. Accordingly, the passgate comprising
transistors 48 and 50 of first latch circuit 16 (Figure
3) passes the first row address into the latch formed
by inverters 52 and 54 (also Figure 3). At the end of
the pulse, $\Phi 1$ signal 78 goes high and the first row
address is latched into the latch of inverters 52 and

54. While the first row address is held in first latch
circuit 16, $\Phi 2$ signal 80 goes low, thereby causing the
passgate comprising transistors 56 and 58 of second
latch circuit 18 (Figure 3) to pass the first row
5 address into the latch formed by inverters 60 and 62
(also Figure 3). At this point, the first row address
is available for decoding by first and second stage row
decoders 20 and 22 (Figure 1). When $\Phi 2$ signal 80 goes
high, the first row address is latched into second
10 latch circuit 18 so that such address may continue to
be decoded. First latch circuit 16 is now available to
receive a second row address.

In another exemplary period 84, a second row
address is set up when the value of $\overline{\text{RAS}}$ signal 72 is
15 high as the value of $\overline{\text{OE}}$ signal 74 transitions low. In
this instance, t_{ORS} is the difference in time between
the moment that $\overline{\text{RAS}}$ signal 72 goes high and the moment
that $\overline{\text{OE}}$ signal 74 goes low. t_{ORH} is the difference in
time between the moment that $\overline{\text{OE}}$ signal 74 goes low and
20 the moment that $\overline{\text{OE}}$ signal 74 goes high again. The
time during which $\overline{\text{RAS}}$ signal 72 is high constitutes the

RAS pre-charge time (t_{RP}). t_{ASR} is the difference in time between the beginning of the second row address and the moment that \overline{OE} signal 74 goes low. t_{RAH} is the difference in time between the moment that \overline{OE} signal 74 goes low and the end of the second row address.

During period 84, at least initially, the first row address may still be decoded even as the second row address is being set up. The transition of \overline{OE} signal 74 from high to low while \overline{RAS} signal 72 is high causes a pulse in $\Phi 1$ signal 78. During such pulse, the value of $\Phi 1$ signal 78 is low so that the passgate of first latch circuit 16 passes the second row address into the latch of the same circuit. At the end of the pulse, $\Phi 1$ signal 78 goes high and the second row address is latched into the latch of inverters 52 and 54. While the second row address is held in first latch circuit 16, $\Phi 2$ signal 80 goes low, which causes the passgate of second latch circuit 18 to pass the second row address into the latch formed by inverters 60 and 62.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations

can be made therein without departing from the spirit
and scope of the invention as defined by the appended
claims.

WHAT IS CLAIMED IS:

1. A circuit for controlling the set up of a memory address, comprising:

5 a first latch circuit for latching a first memory address in response to a first simultaneous occurrence of a predetermined value for an output enable signal and a predetermined value for a row address strobe signal;

10 a second latch circuit coupled to the first latch circuit, the second latch circuit for receiving the first memory address from the first latch circuit and latching the first row address thereafter for decoding; and

15 wherein the first latch circuit latches a second memory address in response to a second simultaneous occurrence of the predetermined value for the output enable signal and the predetermined value for the row address strobe signal, the second simultaneous occurrence occurring while the first row address is
20 being decoded.

2. The circuit of Claim 1, wherein each of the first latch circuit and the second latch circuit comprises:

a passgate responsive to the simultaneous occurrence of the predetermined value for the output enable signal and the predetermined value for the row address strobe signal; and

a latch coupled to the passgate.

3. The circuit of Claim 2, wherein each passgate comprises:

a p-type transistor for receiving a respective timing signal; and

an n-type transistor coupled with the p-type transistor, the n-type transistor for receiving a complement of the respective timing signal.

4. The circuit of Claim 2, wherein each latch comprises:

a first inverter having an input lead coupled to an output lead of the respective passgate; and

a second inverter having an input lead coupled to an output lead of the first inverter, the second

inverter having an output lead coupled to the input
lead of the first inverter.

5. The circuit of Claim 1, further comprising a
5 buffer coupled to the first latch, the buffer for
buffering an address signal conveying the first row
address and the second row address.

6. The circuit of Claim 1, further comprising a
10 timing generator circuit for generating at least one
timing signal in response to the output enable signal
and the row address strobe signal.

7. The circuit of Claim 1, further comprising at
15 least one row decode circuit coupled to the second
latch circuit, the row decode circuit for decoding the
first and second memory addresses.

8. A method for controlling the set up of a memory address, the method comprising:

latching a first memory address in response to a first simultaneous occurrence of a predetermined value
5 for an output enable signal and a predetermined value for a row address strobe signal;

decoding the first memory address for access to at least one memory cell corresponding to the first memory address; and

10 while the first memory address is being decoded, latching a second memory address in response to a second simultaneous occurrence of the predetermined value for the output enable signal and the predetermined value for the row address strobe signal.

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9. The method of Claim 8, further comprising generating at least one timing signal in response to the output enable signal and the row address strobe signal.

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10. The method of Claim 8, further comprising buffering an address signal which conveys the first row address and the second row address.

CONTROLLING THE SET UP OF A MEMORY ADDRESS

Adrian E. Ong

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ABSTRACT OF THE DISCLOSURE

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A circuit is provided for controlling the set up of a memory address. The circuit includes a first latch circuit for latching a first memory address in response to a first simultaneous occurrence of a predetermined value for an output enable signal and a predetermined value for a row address strobe signal. A second latch circuit is coupled to the first latch circuit. The second latch circuit receives the first memory address from the first latch circuit and latches the first row address thereafter for decoding. The first latch circuit can latch a second memory address in response to a second simultaneous occurrence of the predetermined value for the output enable signal and the predetermined value for the row address strobe signal, the second simultaneous occurrence occurring while the first row address is being decoded.

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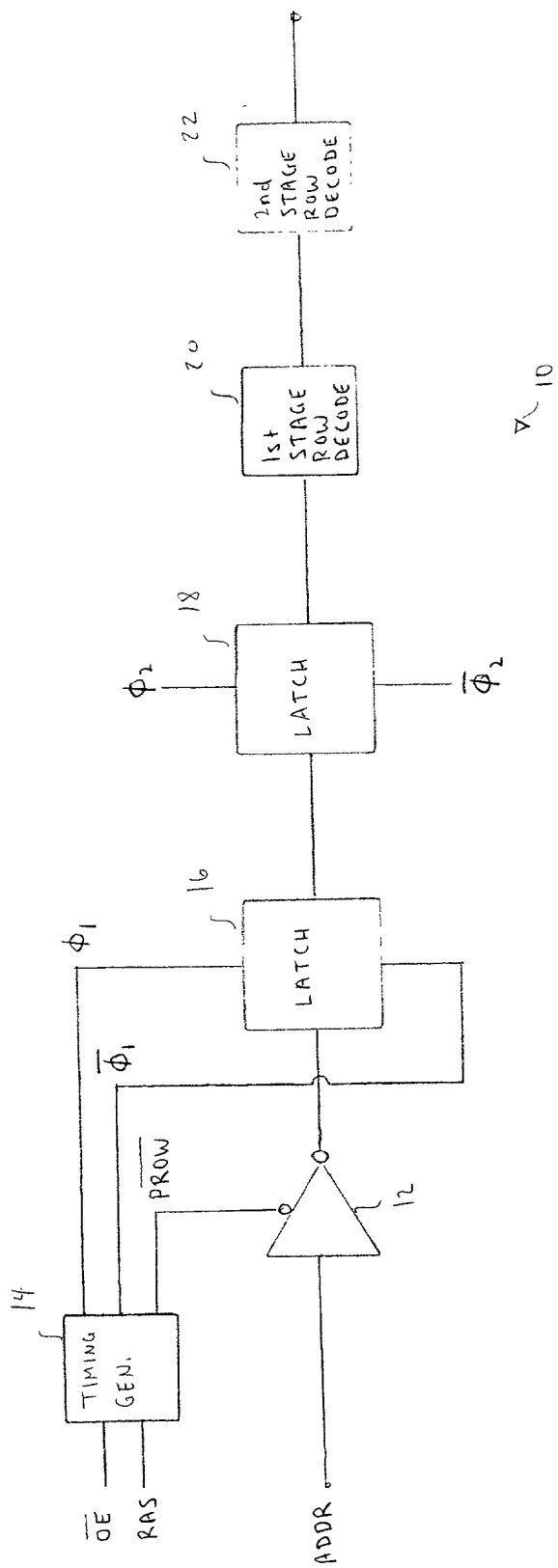


Fig. 1

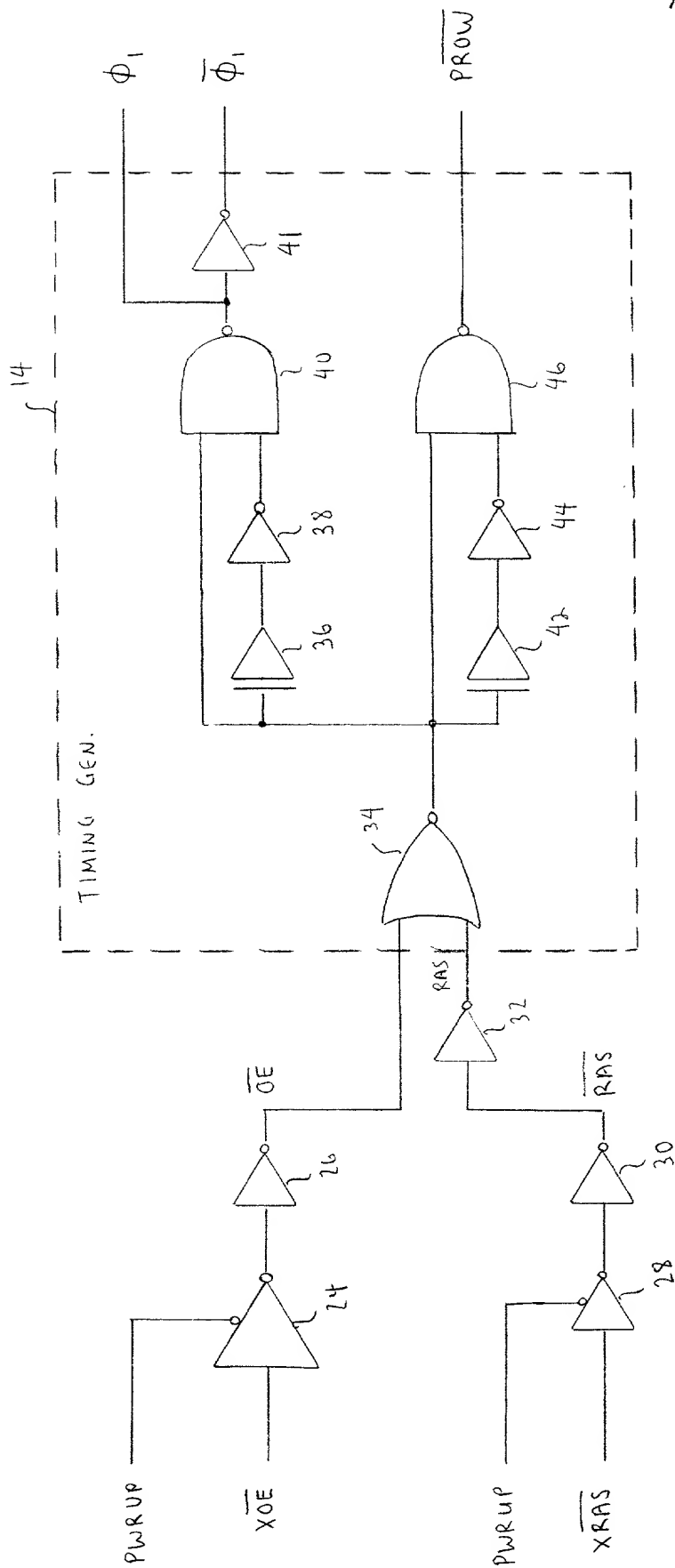


Fig. 2

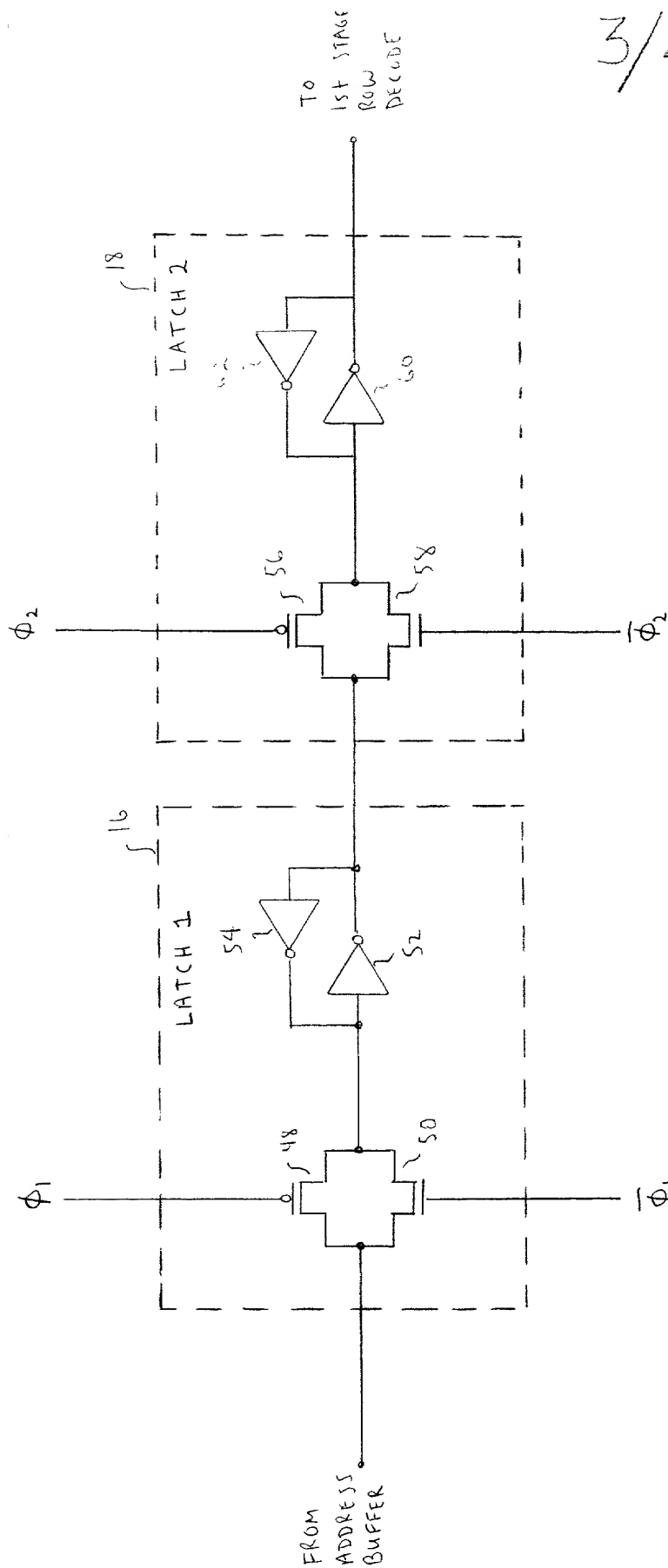


Fig. 3

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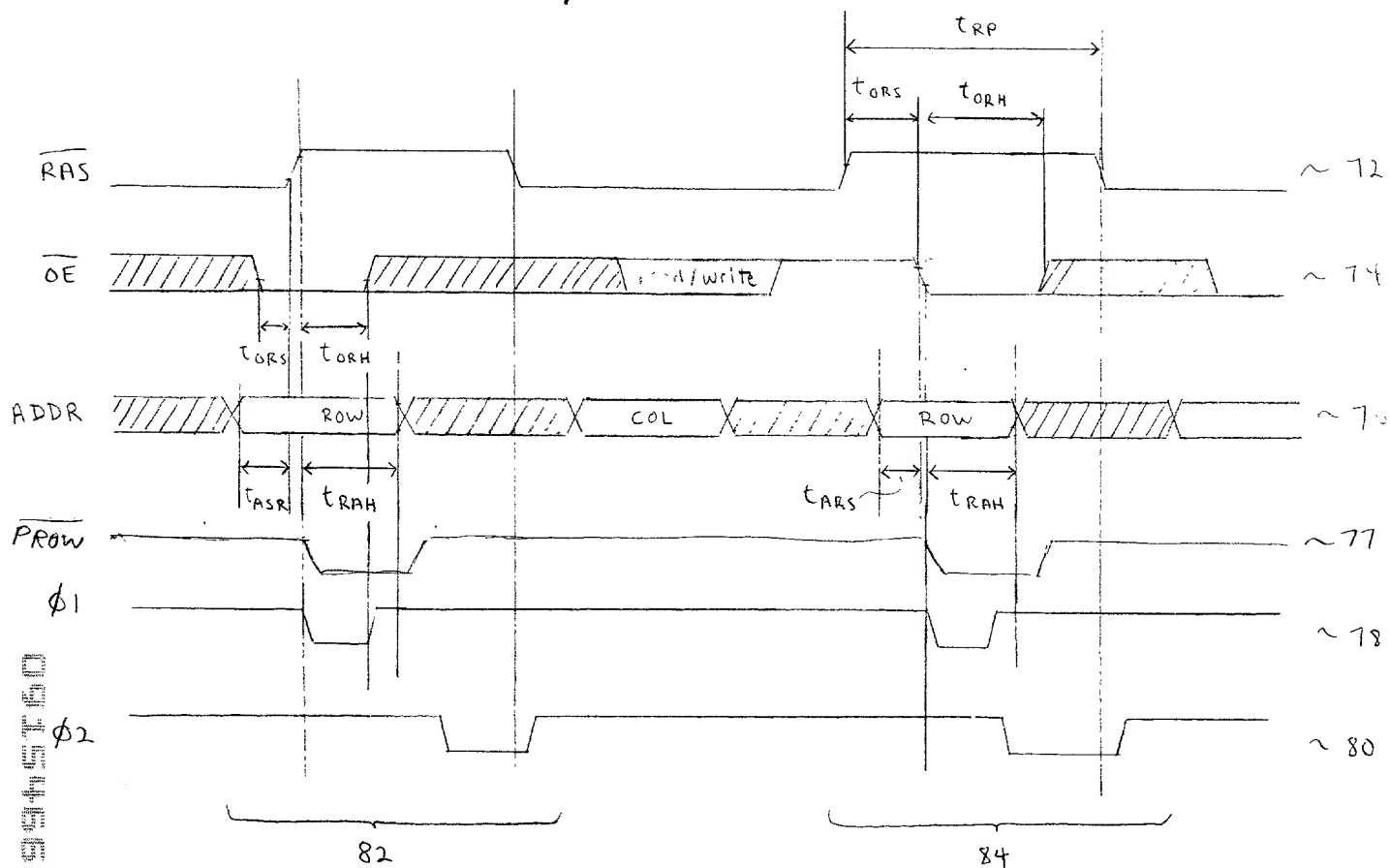


Fig. 4

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DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled Controlling The Set Up Of A Memory Address

which (check) ☒ is attached hereto.

☐ and is amended by the Preliminary Amendment attached hereto.

☐ was filed on _____ as Application Serial No. _____

☐ and was amended on ____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			<input type="checkbox"/>	<input type="checkbox"/>

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Alan H. MacPherson (24,423); Thomas S. MacDonald (17,774); Kenneth E. Leeds (30,566); Brian D. Ogonowsky (31,988); David W. Heid (25,875); Norman R. Klivans (33,003); Edward C. Kwok (33,938); David E. Steuber (25,557); Michael Shenker (34,250); Stephen A. Terrile (32,946); Peter H. Kang (40,350); T. Lester Wallace (34,748); Ronald J. Meetin (29,089); Ken John Koestner (33,004); Omkar K. Suryadevara (36,320); David T. Millers (37,396); Kent B. Chambers (38,839); Serge J. Hodgson (40,017); Michael P. Adams (34,763); Bernard Berman (37,279); Michael J. Halbert (40,633); Gary J. Edwards (41,008); William B. Tiffany (41,347); James E. Parsons (34,691); Daniel P. Stewart (41,332); Philip W. Woo (39,880); John T. Winburn (26,822); Tom Chen (42,406); Fabio E. Marino (43,339); William W. Holloway (26,182); Elaine H. Lo (41,158); and Don C. Lawrence (31,975).

Please address all correspondence and telephone calls to:

Alan H. MacPherson
Attorney for Applicant
SKJERVEN, MORRILL, MacPHERSON, FRANKLIN & FRIEL LLP
25 Metro Drive, Suite 700
San Jose, California 95110-1349

Telephone: 408-453-9200
Facsimile: 408-453-7979

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

Full name of sole (or first joint) inventor: Adrian E. Ong

Inventor's Signature: Adrian E. Ong

Date: 9/8/98

Residence: Pleasanton, California

Post Office Address: 2770 Huff Drive
Pleasanton, CA 94588

Citizenship: Singapore

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Adrian E. Ong
Assignee: G-Link Technology
Title: CONTROLLING THE SET UP OF A MEMORY ADDRESS
Serial No.: Unknown Filed: Herewith
Examiner: Unknown Group Art Unit: Unknown
Docket No.: M-5961 US

San Jose, California

BOX PATENT APPLICATION
COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

**SMALL BUSINESS CONCERN
DECLARATION BY ASSIGNEE**

Dear Sir:

I declare that I am an official empowered to act on behalf of the concern identified above as assignee.

Exclusive rights to the above invention as described in

- ☒ the specification filed herewith,
☐ U.S. patent application Serial No. , filed

have been conveyed to and remain with the above concern.

For purposes of paying reduced fees under Section 41 of Title 35 of the United States Code with regard to this invention, I declare that the above concern qualifies as a small business concern as defined in 13 CFR 121.12 and reproduced in 37 CFR 1.9(d), namely, the concern's number of employees, including those of its affiliates, does not exceed 500 persons and the concern has not assigned, granted, conveyed, or licensed, and is under no obligation

under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

I acknowledge my duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate per 37 CFR 1.28(b).

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

Signature: _____

Steve Ou

Date: _____

9/10/98

Official's Name: _____

Steve Ou

Official's Title: _____

President

Concern's Name: _____

G-Link Technology

Concern's Address: _____

2701 Northwestern Parkway
Santa Clara, California 95051